

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
MATHEW, LEO, et al.

Application No.: 10/695163

Filed: 10-28-2003

Docket No.: SC12746TP

§ Patent No.: 6951783 B2

§ Issue Date: 10-04-2005

§ Examiner: Trung Dang

§ Group Art Unit: 2823

Title: CONFINED SPACERS FOR DOUBLE GATE TRANSISTOR SEMICONDUCTOR
FABRICATION PROCESS

Certificate of Submission

I hereby certify that this correspondence is being submitted to the USPTO,
Alexandria, VA.

Addressed per C.F.R. § 1.1(a) and deposited with the United States Postal
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2/11/08
Date of Submission

Signature

PAT THOMAS
Printed Name of Person Signing Certificate

Commissioner for Patents
Alexandria, VA 22313

SUBMISSION OF CERTIFICATE OF CORRECTION

Dear Commissioner:

Enclosed is a Certificate of Correction listing error(s) in the subject patent.

Please enter these corrections. Since the errors appear to be on the part of the United
States Patent Office, there should be no charge.

2008-02-08
Date

Respectfully submitted,

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CERTIFICATE OF CORRECTION

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PATENT NO.: 6951783 B2
APPLICATION NO: 10/695163
DATE: 10-28-2003
FIRST NAMED INVENTOR: MATHEW, LEO

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Column 8, Line 64, Claim No. 16:

Change "overlaying" to --overlying—

In Column 9, Line 5, Claim No. 16:

Change "within fin underlying" to -- within the silicon fin underlying--

MAILING ADDRESS OF SENDER (Please do not use customer number below)

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